SESSION 16 – HONOLULU SUITE
Digital Techniques I

Friday, June 18, 1:30 p.m.
Chairpersons: S. Kosonocky, IBM
N. Lu, Etron

16.1 — 1:30 p.m.
Analysis and Design of Transceiver Circuit and Inductor Layout for Inductive Inter-Chip Wireless Superconnect, N. Miura, D. Mizoguchi, Y.B. Yusof, T. Sakurai* and T. Kuroda, Keio University, Yokohama, Japan, *The University of Tokyo, Japan

A wireless bus for stacked chips was developed by utilizing inductive coupling. This paper discusses inductor layout optimization and transceiver circuit. Testchip was fabricated in 0.35um CMOS. Accuracy of the models is verified. BER is investigated for various inductor layouts and communications distance. Transceiver achieved 1.25Gb/s/channel inter-chip communication with power dissipation of 45.6mW. If chip thickness is reduced to 30um in 90nm device generation, power dissipation will be 1mW/channel or bandwidth will be 1Tb/s/mm2.

16.2 — 1:55 p.m.
An On-Die CMOS Leakage Current Sensor for Measuring Process Variation in Sub-90nm Generations, C.H. Kim, K. Roy, S. Hsu*, R.K. Krishnamurthy* and S. Borkar*, Purdue University, West Lafayette, IN, *Intel Corporation, Hillsboro, OR

This paper describes an on-die leakage current sensor in 1.2V, 90nm CMOS technology for accurately measuring process variation. Results based on measured leakage data show (i) higher signal-to-noise ratio and (ii) reduced sensitivity to supply and P/N skew variations compared to prior designs, while the proposed sensor only requires a single bias generator even for multi-bit resolution sensing. A 6-channel leakage current monitor testchip fabricated in 90nm dual-Vt CMOS is also described.

16.3 — 2:20 p.m.
High-Resolution On-Chip Propagation Delay Detector for Measuring Within-Chip and Chip-to-Chip Variation, T. Matsumoto, Fujitsu Laboratories, Ltd., Tokyo, Japan

We propose a circuit that can measure the propagation delay of a logic circuit directly even for one fan-out 1 inverter of CMOS 90 nm node technology. We obtained high-resolution (1 ps) by converting the propagation delay to the control voltage of the voltage-controlled delay line in Delay-Locked Loop. The circuit was fabricated with 90 nm CMOS technology. This circuit can be used for measuring within-chip variation that is important for future design automation.

16.4 — 2:45 p.m.
A 233MHz, 80-87% Efficient, Integrated, 4-Phase DC-DC Converter in 90nm CMOS, P. Hazucha, G. Schrom, J.-H. Hahn, B. Bloechel, P. Hack, G. Dermer, S. Narendra, D. Gardner, T. Karnik, V. De and S. Borkar, Intel Laboratories, Hillsboro, OR

We demonstrate an integrated buck DC-DC converter implemented in a 90nm CMOS technology for multi-Vcc microprocessors. High switching frequency (100-317MHz), 4-phase topology, and fast hysteretic control reduce inductor and capacitor sizes by 1000x, thereby enabling off-chip inductors with no magnetic core and an on-chip decoupling capacitor. The converter achieves 80-87.7% efficiency and 10% peak-to-peak output noise.

Break 3:10 p.m.